

**AMENDMENTS TO THE DRAWINGS**

Please replace the current version of Figure 5 with the drawing sheet attached to this Amendment.

**REMARKS**

The Examiner's Office Action mailed on January 18, 2005 has been received and its contents carefully considered.

Claims 1-8 are pending in this application. Claim 4 is amended herein. Claims 1, 4 and 5 comprise the independent claims.

In the Action, the Examiner has objected to Figure 5 of the drawings on the grounds that the figure should be designated by the legend such as --Prior Art-- because only that which is old is illustrated. In response, Figure 5 is corrected herein to include such a legend. The Examiner's review and approval of the corrected drawing, which is attached to this Amendment, are respectfully requested.

In the Action, claim 4 is rejected under 35 USC §112, first paragraph, as failing to comply with the written description requirement. The Examiner asserts that the claim contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the in relevant art that the inventor(s), of the time the application was filed, had possession of the claimed invention. Specifically, the Examiner points to claim 4 as containing the limitation of read-out selection means for selecting the connection information from one of the switching memory means and the information receiving means (page 6, line 10-12 of amendment dated May 5, 2004), for which the Examiner could not find support in the specification.

Claim 4 is amended here in to overcome the §112 rejection. Specifically, the term "switching memory means" in the above-cited limitation, is replaced by --working memory means-- in order to correct a clerical error made when claim 4 was amended in the above-mentioned amendment of May 5, 2004. As now amended, claim 4 is clearly supported by Figure 6 of the application and the accompanying description beginning on page 22, line 9 of the application. The Examiner's entry of amended claim 4 and withdrawal of the §112, first paragraph, rejection are respectfully requested.

The Applicants note that claim 4 is directed to a configuration using a single working memory, which is significantly different from Murata. Figure 7 of Murata discloses the use of two RAM memories 12 and 13 that are the same. In Murata, the connecting information after switching is stored in an unselected control memory that is either memory 12 or 13, and the roles of the memories are exchanged. On the other

hand, Figure 6 of the present application shows the claimed working memory, which advantageously has a lower capacity, i.e., sufficient for just one time switching. Thus, it is respectfully submitted that claim 4 patentably distinguishes over the Murata reference.

In the Final Action, claims 1-3 and 5-8 are rejected under 35 U.S.C. §102(b) as being anticipated by Murata et al. (U.S. Patent No. 4,759,010). The rejection is respectfully traversed.

Anticipation under 35 U.S.C. §102 requires that each element of the claim in issue be found, either expressly described or under principles of inherency, in a single prior art reference. Although anticipation requires only that the claim under attack "read on" something disclosed in the reference, all limitations of the claim must be found in the reference, or "fully met" by it.

With regard to claim 1, the Examiner points to Murata as teaching all of the features and limitations of the claimed invention. The Applicants respectfully disagree. For example, claim 1, requires "switching memory means for storing and switching data of the time slots from the multiplexing means, for one frame period" (emphasis added). The Examiner cites no specific section of Murata as teaching or suggesting the limitation "for one frame period." To the contrary, Murata discloses with reference to Figure 3 that the switching memory comprises two memories, such that the first memory 250 successively writes the data inputted from the terminal 201 according to the sequential addresses outputted via said selector 230 (speech data write mode), and in the meantime, the second memory 260 reads out data written in the previous one frame according to the address from the selector 240 (speech data read mode), and it is supplied to the selector 270, which outputs this read data to an output terminal 205). In the next frame, the frame pulse FP is supplied to the control logic circuit 220 to invert the selection signal, and an operation inverse to the foregoing is done (column 4, lines 14-24). Thus, is clear that in Murata, the switching memory stores two frames of speech data, rather than the single frame recited in the claims.

Further, claim 1 requires "information receiving means for receiving connection information from the upper layer controller" (emphasis added). The section of Murata relied upon by the Examiner as teaching this limitation (column 6, lines 45-49)

discloses only that the signal that the address signal ADR is supplied from the path controller 40 into the address register 113 via the terminal 103, and the control dated D to be written into that address is fed at the same time to the data register 112 via the terminal 102. Murata fails to teach or suggest that the path controller 40 is an "upper layer controller," as that term would be understood by one of ordinary skill in the art.

Thus, for at least the reasons discussed above, it is respectfully submitted that claim 1, as well as claims 2-8, patentable distinguish over the applied prior art.

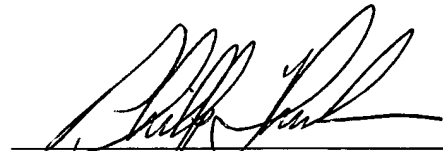
In summary, it is submitted that this Amendment places the application in condition for allowance. Withdrawal of the final rejections and entry of this Amendment are respectfully requested.

Should the Examiner feel that a conference would help to expedite the prosecution of this application, the Examiner is hereby invited to contact the undersigned counsel to arrange such an interview.

Respectfully submitted,

April 18, 2005

Date



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Attachment

- Replacement Drawing Sheet (Fig. 5)